DATA SHEET

PCF2042 V2
Memory card IC

Product Specification (Rev. 1997 Feb 03) 1997 Feb 03

Philips
Semiconductors

PHILIPS

CONTENTS

Note: For mechanical information see separate documents
“Wafer Specifications for Chip Card ICs” and
“Module Specifications for Chip Card ICs”

1 FEATURES

- Memory size of 256 x 8-bit EEPROM
- Byte-wise addressing of information
- Irreversible byte-wise write protection of 32 bytes of main memory
- Two-wire link protocol
- Answer to RESET according to ISO 7816-3
- Programming time per byte 2.5 ms for erasing and 2.5 ms for writing
- Minimum of 10^5 erase/write cycles
- Data retention 10 years (min)
- Contact configuration and serial interface according to ISO 7816 (synchronous transmission)
- CMOS technology
- Data can only be changed after entry of the correct 24-bit verification data for the programmable security code (Security Memory)
- 5 kV ESD-protection (Human Body model)
- FabKey procedure

2 GENERAL DESCRIPTION

The PCF2042 contains a 256 x 8-bit EEPROM with programmable write protection for each of the first 32 bytes. Reading of the whole memory is always possible. The memory can be written and erased byte by byte.

Each of the first 32 bytes can be write/erase protected by setting a Protection bit (EEPROM converted to ROM). If set once, the Protection bit cannot be erased.

Additionally, the PCF2042 allows for a verification procedure. The whole memory, excluding the Reference Data, can be read always. The memory can be written or erased only after a successful comparison of the verification data.

After three successive incorrect entries an internal error counter will block any subsequent attempt to compare the verification data, and hence blocks any possibility to write and erase.

3 ORDERING INFORMATION

For details contact your local Philips Organisation.

TYPE NUMBER	PACKAGE		TEMPERATURE RANGE (°C)
	NAME	DESCRIPTION	
PCF2042 U	wafer	5” wafer, unsawn; note 1	-40 to +85
PCF2042 V	module	6- or 8-contact Modules on 35 mm film; note 2	
PCF2042 W	FFC	sawn wafer on film frame carrier 6” or 7”; note 1	

Notes

1. See “Wafer Specifications for Chip Card ICs”.
2. See “Module Specifications for Chip Card ICs”.

4 BLOCK DIAGRAM

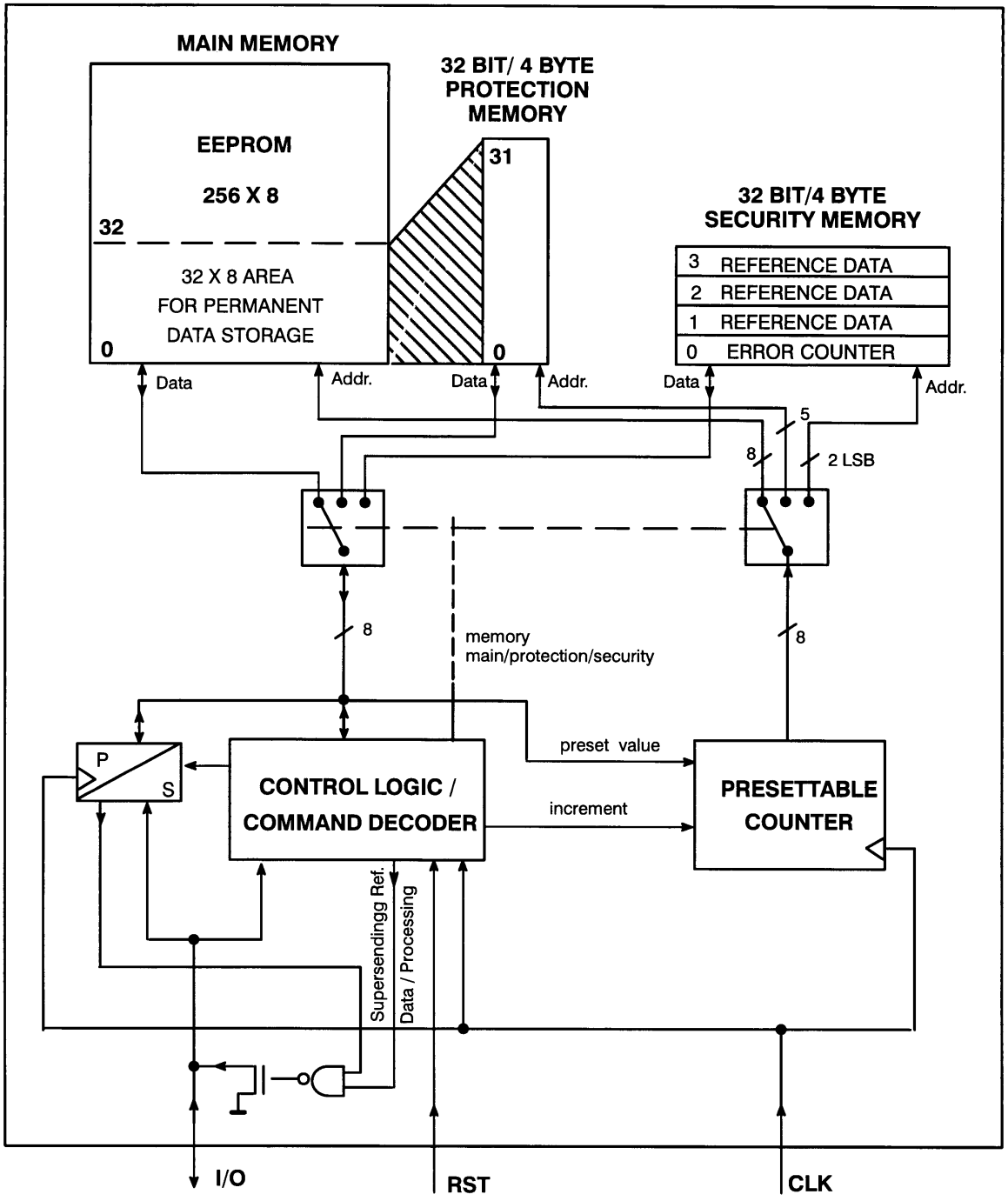

Fig.1 Block diagram PCF2042.

5 MEMORY CONFIGURATION

The IC contains 256 byte EEPROM of Main Memory, divided into a protected and main area. The protected Memory of 32 byte is located at the first address locations of the main area with the remaining 224 bytes. All protectable bytes have associated Protection bits (32 bit/4 byte). In addition to this memory mapping the PCF2042 is provided with a separate Security Memory of 32 bit/4 byte.

All bytes of the three memory areas can always be read out, except of the Reference Data. When the command “Read Security Memory” is applied before write access to all memories has been enabled, the Reference Data are superseded by 0x00.

Generally, the write access to all memories is protected by a 24-bit/3 byte Reference Data. After a successful comparison with the Verification Data (see section 5.4.4) the write access to Main Memory, Protection Memory and Security Memory as well as read-out of the reference data is enabled.

The Error Counter counts the number of failed comparisons of Verification/Reference Data. Only the last three bits are significant. The five higher bits are permanently LOW.

The Protection bits are used to inhibit alteration of data stored in the first 32 bytes of the Main Memory. The two states of the Protection bits are defined as:

HIGH = Write enabled

LOW = Write disabled

When a Protection bit has been programmed to LOW a reset of that bit to HIGH is inhibited. Thus, information stored in the first 32 bytes of the Main Memory are protected against any alteration.

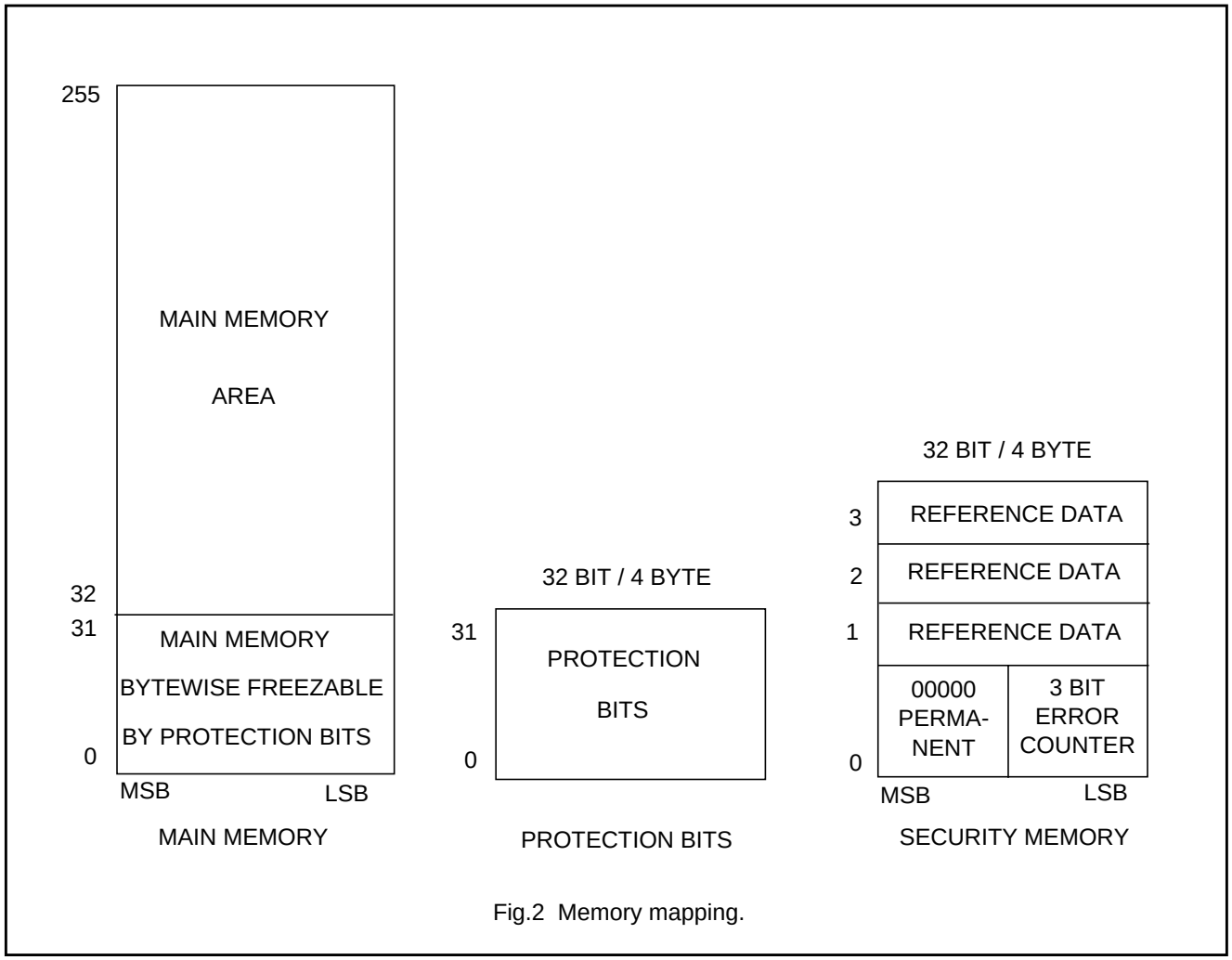

Fig.2 Memory mapping.

5.1 Transmission Protocol

The transmission protocol is a two-wire link protocol and is identical to the protocol type S=10 for synchronous transmission. The characteristics of synchronous transmission are part of ISO 7816-3.

All data changes on I/O are initiated by the falling edge of CLK.

5.1.1 RESET AND ANSWER-TO-RESET (ATR)

Reset of the IC complies with the synchronous parts of ISO 7816-3. The RESET can be given at any time during operation. The first 32 clock pulses will provide the Answer-to-Reset. (For details see Chapter 7.)

The IC discards any START/STOP condition during ATR.

After having read the last bit an additional clock pulse is mandatory in order to set I/O to HIGH.

Any further clock that follows now will not change the level on I/O.

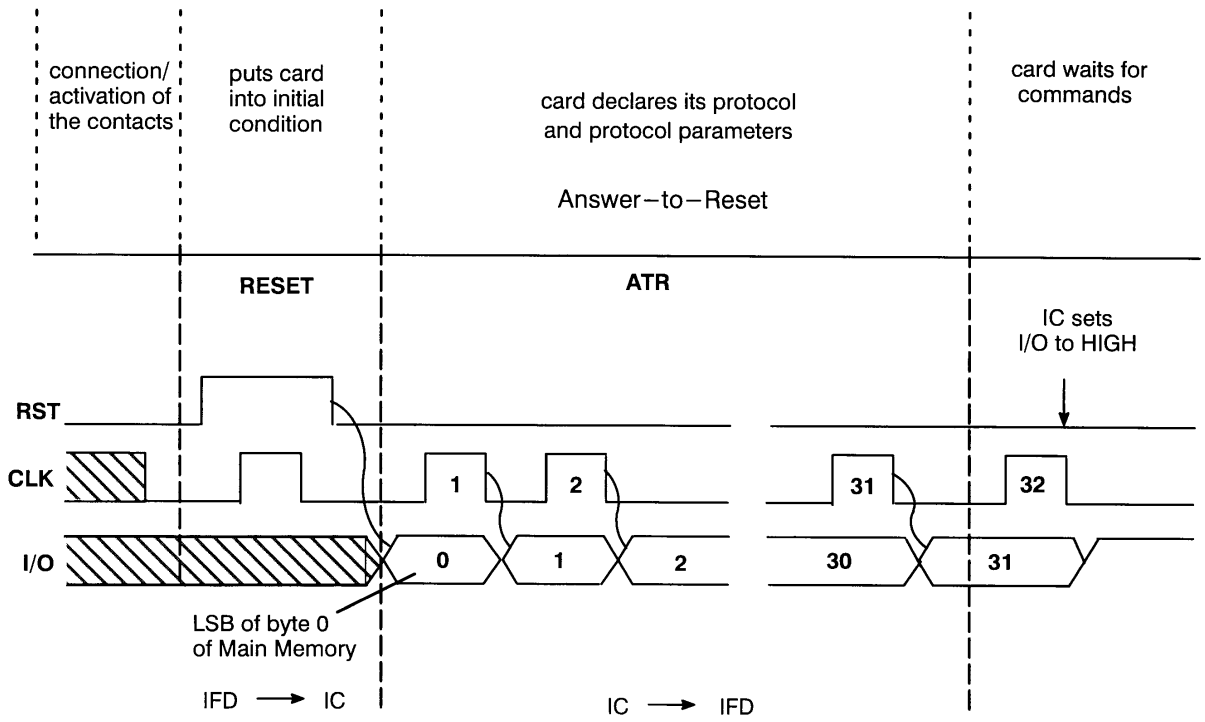

Fig.3 The activation, RESET and Answer-To-Reset phase.

5.1.2 COMMAND MODE - IFD TO IC

Any bit sequence transmitted from the interface device (IFD) to the IC is embedded between a START condition and a STOP condition:

START condition:

- falling edge on I/O during CLK is HIGH

STOP condition:

- rising edge on I/O during CLK is HIGH

Between the last bit of a bit sequence transmitted from IFD to IC and the STOP condition, an additional clock pulse is mandatory in order to set I/O to HIGH.

If not exactly 24 bits are transmitted from IFD, the IC responds with processing mode.

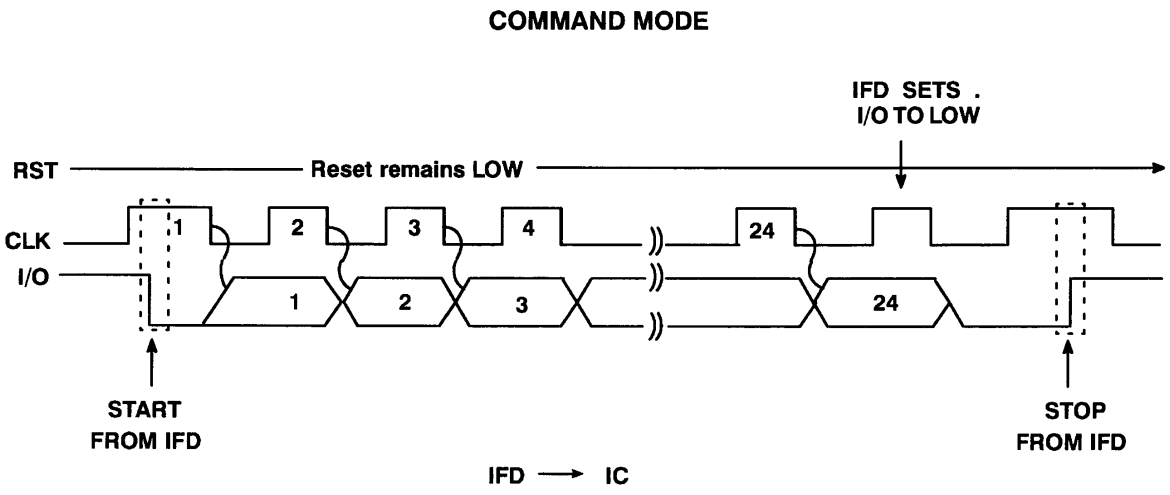

Fig.4 The command phase.

5.1.3 OUTGOING DATA/PROCESSING MODE - IC TO IFD

After the transmission of a bit sequence from interface device (IFD) to IC, two operational modes of the IC are to be distinguished.

5.1.3.1 Processing Mode

- In this mode the IC is processing internally. No data bits are sent.
- During processing the IC has to be clocked continuously by the IFD. In this phase the I/O is set to LOW by the IC. The IC signals the end of its internal processing by setting I/O to HIGH.
- The IC discards any START/STOP condition during processing mode.
- Any further clock that follows when processing mode is completed will not change the level on I/O.

The IC only indicates the ‘End of Processing’ to the IFD. The IC provides no information about the result of the ‘processing’.

5.1.3.2 Outgoing Data Mode

- In this mode the IC sends data to the IFD.
- The first data bit becomes valid on I/O after the first falling edge on CLK. After the last outgoing bit from the IC, an additional clock pulse is mandatory in order to set I/O to HIGH. This prepares the IC for a new START condition. Note: The number of outgoing bits is known by the IC and the IFD.
- The IC discards any START/STOP condition during outgoing data mode.
- Any further clock that follows when outgoing data mode is completed will not change the state on I/O.

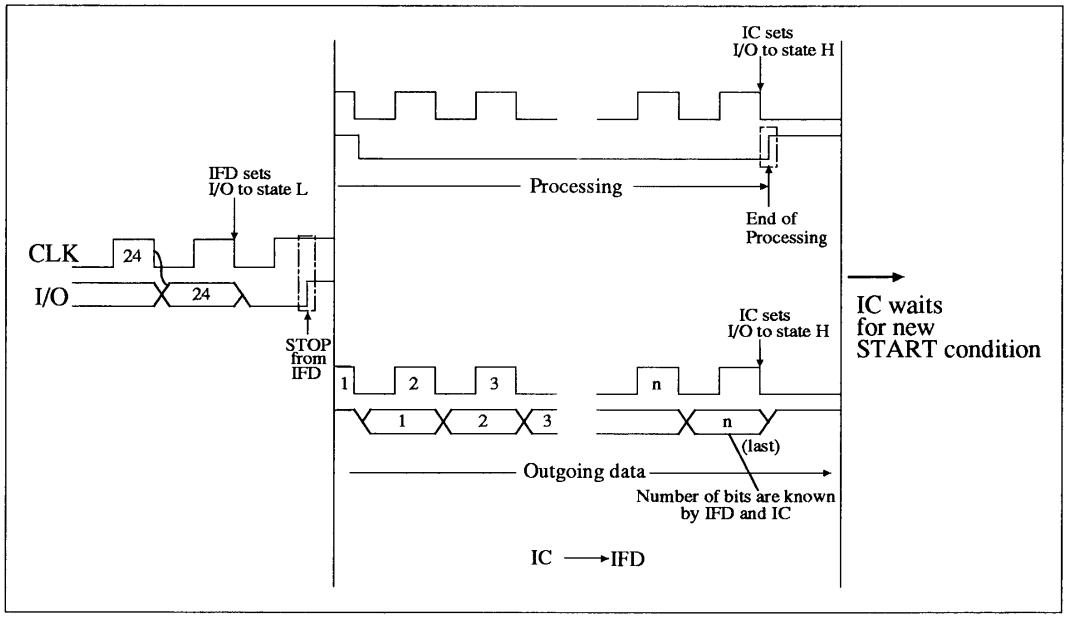

Fig.5 The Output/Processing Mode

5.2 Clock

The frequency delivered by the IFD on CLK shall be in the range of 7 kHz to 50 kHz with a duty cycle between 40% and 60%. When switching frequencies, no pulse shall be shorter than 40% of the shorter period.

5.3 Command format

Each command consists of three bytes. The first byte (Control byte) defines the command to be executed. The second one defines the address in the EEPROM memory and the third one contains the Data byte.

Table 1 Command format

The LSB of transmitted bytes is always send first.

CONTROL BYTE		BYTE ADDRESS		DATA BYTE	
MSB	LSB	MSB	LSB	MSB	LSB

Table 2 Coding of commands

The control byte is coded according to the table below.

CONTROL BYTE MSB / LSB	BYTE ADDRESS	DATA BYTE	COMMAND	MODE
0011.0000	0x00-0xFF	xx	READ MAIN MEMORY	outgoing
0011.0001	xx	xx	READ SECURITY MEMORY	outgoing
0011.0010	--	--	not defined	processing
0011.0011	0x01-0x03	byte 1-3	COMPARE VERIFICATION DATA	processing
0011.0100	xx	xx	READ PROTECTION MEMORY	outgoing
0011.0101	--	--	not defined	processing
0011.0110	--	--	not defined	processing
0011.0111	--	--	not defined	processing
0011.1000	0x00-0xFF	data byte	UPDATE MAIN MEMORY	processing
0011.1001	0x00-0x03	data byte	UPDATE SECURITY MEMORY	processing
0011.1010	--	--	not defined	processing
0011.1011	--	--	not defined	processing
0011.1100	0x00-0x1F	data byte	WRITE PROTECTION MEMORY	processing
0011.1101	--	--	not defined	processing
0011.1110	--	--	not defined	processing
0011.1111	--	--	not defined	processing

Any faulty input condition from IFD to IC will force the following response after the stop condition:

- the IC responds with processing mode,
- the IC sets I/O to HIGH after 8 falling edges of CLK.

5.4 Description of Commands

5.4.1 Read Main Memory

The READ MAIN MEMORY command reads out the content of the Main Memory starting at the given byte address up to the end of the memory (address 255). The read access to the Main Memory is always possible.

5.4.2 Read Protection Memory

The READ PROTECTION MEMORY command reads out the Protection Memory starting at address 0x00 up to the end of the memory (address 0x03). The read access to the Protection Memory is always possible.

5.4.3 Read Security Memory

The READ SECURITY MEMORY command reads out the Security Memory starting at address 0x00 up to the end of the memory (address 0x03). The read access to the Security Memory is always possible.

The actual value of the Reference Data can only be read after a 'Write Access procedure' has been carried out successfully. Otherwise the Reference Data are superseded by 0x00.

5.4.4 Compare Verification Data

The purpose of this command is to achieve write access to all three memories, the Protection Memory, the Security Memory and the Main Memory.

Verification Data will be sent to the IC being internally compared with the Reference Data. Furthermore, the COMPARE VERIFICATION DATA command must be used together with the Error Counter byte within the 'Write Access Procedure' (see Fig.6).

As long as the full write access to the system is not given, the content of the Error Counter can only be changed from HIGH to LOW. Thus, single bit changes of the Error Counter allow at three attempts to achieve the full write access to the system using the 'Write Access Procedure'. If the 'Write Access Procedure' ends successfully, full write access to the Error Counter is given also.

To achieve the full write access, first the Error Counter at address 0x00 has to be written. Subsequently, all three Reference Data bytes (Security Memory address: 0x01,0x02,0x03) have to be addressed using the COMPARE VERIFICATION DATA command in the sequence of increasing addresses starting with Reference Data byte 1. Any command given in between these three COMPARE VERIFICATION DATA commands will result in a failure of the 'Write Access Procedure'.

Any single COMPARE VERIFICATION DATA command with mismatching byte between Verification and Reference Data will abort the 'Write Access Procedure'.

Failing the 'Write Access Procedure' when all three bits of the Error Counter are LOW will forever disable any further write access.

If wrong addresses (undefined or not-ascending) of the Reference Data bytes or Error Counter are transmitted, the 'Write Access Procedure' will fail.

The Data byte transmitted to set the Error Counter byte shall only initiate transitions from HIGH to LOW of the Error Counter bits. Otherwise the 'Write Access Procedure' fails.

If not exactly 24 bits are transmitted from IFD, the IC responds with processing mode and the 'Write Access Procedure' fails.

The number of clock cycles has to be identical for successful/failing COMPARE VERIFICATION DATA command.

A granted write access gets only disabled by a Power-off / Power-on sequence.

Note:

On successful completion of the "Write Access Procedure" the Error Counter should be reset by the IFD to ensure again three attempts after another Power-off/Power-on sequence.

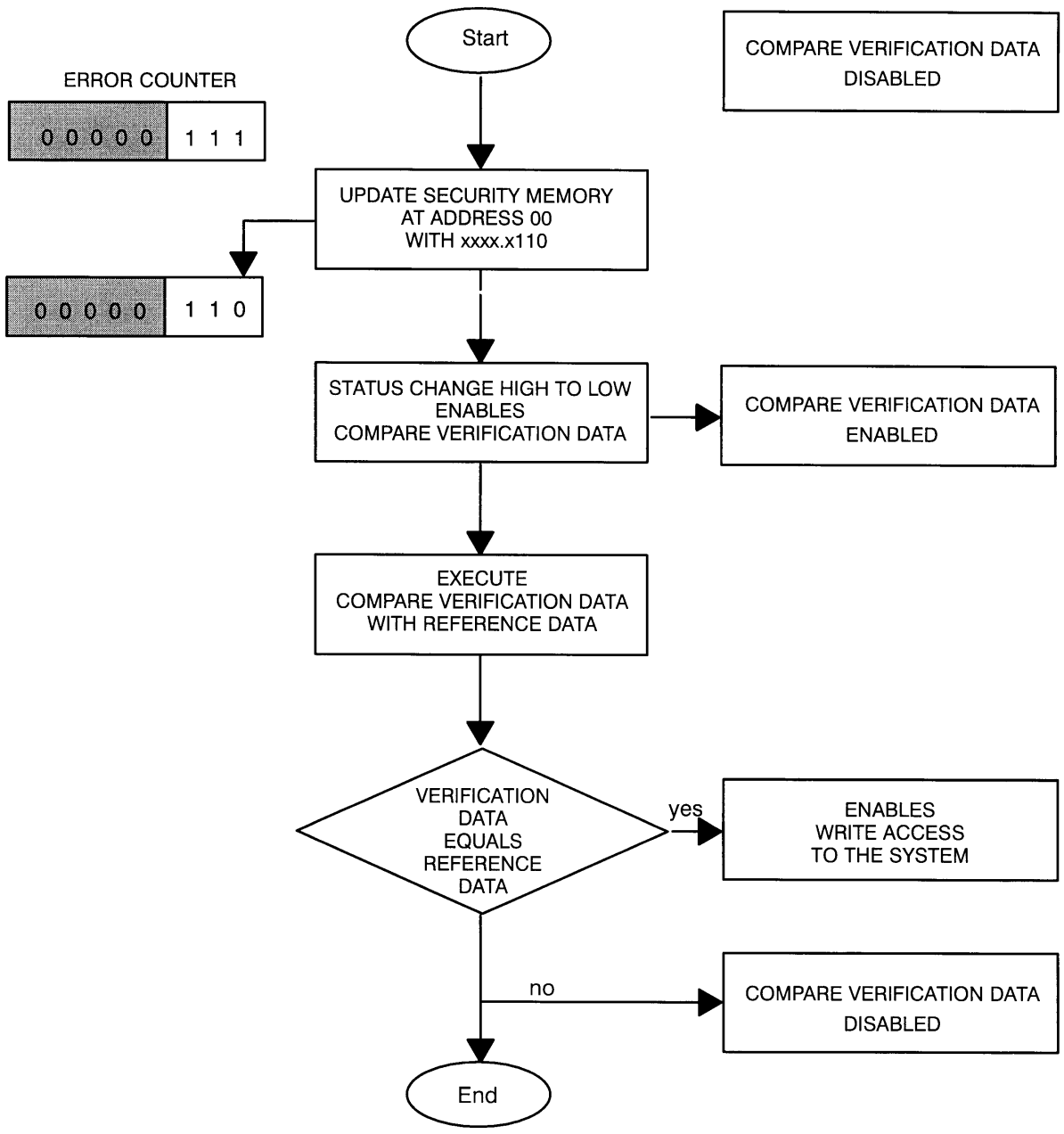

Fig.6 The “Write Access Procedure”.

5.4.5 UPDATE/WRITE COMMANDS

The EEPROM programming is defined as:

Erase: change EEPROM byte from 0xXX to 0xFF

Write: change EEPROM bits from HIGH to LOW (no changes from LOW to HIGH)

All other data changes require a complete Erase- and Write-cycle.

If the data byte transmitted equals the current content of the addressed EEPROM byte, neither the Erase- nor the Write-cycle will be executed.

The Erase-cycle as well as the Write-cycle takes 2.5 ms each.

Before any data can be programmed at least one of the read commands or Answer-to-Reset must be given.

5.4.6 UPDATE MAIN MEMORY

The UPDATE MAIN MEMORY command programs the EEPROM cell addressed by ‘byte Address’ with the Data byte transmitted.

The write attempt fails, if the addressed byte has been protected by the appropriate Protection bit.

5.4.7 WRITE PROTECTION MEMORY

The WRITE PROTECTION MEMORY command programs the EEPROM protection bit addressed by ‘byte Address’, only if the Data byte transmitted equals the data content of the EEPROM byte to be protected. If the transmitted data byte does not match, the Protection bit will not be set.

If the transmitted address is greater than 0x1F, the command is ignored.

5.4.8 UPDATE SECURITY MEMORY

The UPDATE SECURITY MEMORY command programs the EEPROM cell addressed by ‘byte Address’ with the data byte transmitted.

If the transmitted address is greater than 0x03, the command is ignored.

6 RESET MODES

6.1 Reset

If RST is set to HIGH for at least 5 μs and if the IFD keeps CLK in low state during the reset pulse, the IC aborts any operation, sets the I/O line to HIGH and is then ready for further operations.

6.2 Answer-To-Reset

The Answer-to-reset is initiated according to ISO standard 7816-3. The four data bytes of the ATR are serially output to I/O with LSB first when 32 clock pulses are applied to CLK. The I/O is set to HIGH after an additional clock pulse (see Fig.3 and Chapter 5).

6.3 Power on Reset

After applying the operating voltage VCC, the I/O goes to HIGH. Before any data can be programmed at least one of the read commands or Answer-to-Reset must be given.

7 APPLICATION INFORMATION

- Personalization of Memory Card ICs

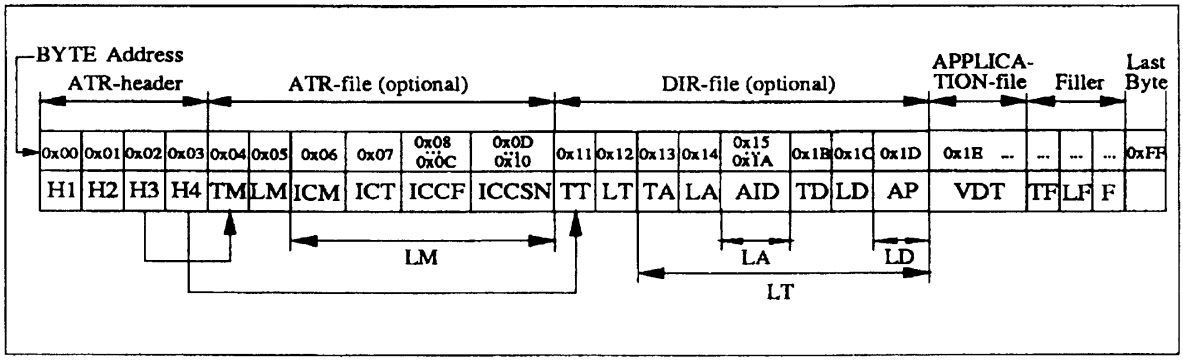

Fig.7 ATR data structure.

Abbreviations used in Figure 7:

AID: Application Identifier
AP: Application Personalizer Identifier
ATR: Answer-To-Reset
DIR: Directory
F: Filler
H1,H2: ATR protocol bytes
H3,H4: ATR historical bytes
ICCF: IC Card Fabricator Identifier
ICCSN: IC Card Serial Number
ICM: IC Manufacturer Identifier
ICT: IC Type
LA: Length of AID
LD: Length discretionary data
LF: Length of Filler
LM: Length manufacturer data
LT: Length application template
TA: Tag of AID
TD: Tag of discretionary data
TF: Tag of Filler
TM: Tag manufacturer data
TT: Tag application template
VDT: 'Versicherten' data template

The following data are unalterably programmed after final production test:

H1, H2, H3, H4, ICM, ICT

7.1 Memory Card ICS

For the memory ICs a normal Answer to Reset (ATR) of 4 x 8 bit is used. The ATR identifies the card to the terminal. The ATR, ATR data and DIR data are programmed into byte 0 to 31 of the EEPROM memory.

All these bytes from address 0 up to address 31 (0x1F) in the memory can be turned into ROM by setting the according protection bits (see Chapter 5).

Once frozen these bytes can not be altered any more!

The memory card ATR looks as follows (see Fig.7):

ATR header:

H1 .. H4	4 bytes, which refer to the ISO 7816, Part 3 standard (address 0 .. 3)
H1 =	protocol (here “0xA2” stands for 2-wire bus protocol/general purpose structure)
H2 =	memory organization, means number of data units and length of data units (e.g. for 2042 -> “13” stands for: 256 x 8 bit)
H3, H4	are the so called historical data as defined in ISO7816, part 3
H3 =	category indicator: DIR data exists Yes/No (here “0x10” = Yes)
H4 =	address of DIR data (here “0x91”, bit 8 set to “1” says address is valid, address = “0x11”, so points to the first byte of the DIR file)

The terminal reads the ATR and if H3 = 0x10, the DIR address is read in H4 and the terminal then jumps to DIR (H1 .. H4 must always be read!).

DIR data:

The whole ATR is TLV (tag/length/value) coded. This means there are always three entries:

Tag	indicates position of any of the entries or identifier, all these tags are given by ISO
Length	gives length of the entry in number of data units (bytes)
Value	is the contents of the entry or identifier

So in the DIR file there is first of all a tag TT for the application template followed by the length (LT), then comes the application identifier (AID), also leaded by the AID-tag (TA) and AID-length (LA). The last part of the DIR file is the application personalizer ID, which also has this structure.

7.2 Application Identifier (AID)

Main reason to have an application specific identifier within every card is that ATR enables to distinguish between different applications, which are using the same protocol, same silicon etc.

So in case the AID is not correct for the applications the card is used for, the terminal should automatically reject the card, so any confusion or abuse get avoided.

The application identifier can be applied at GMD (Gesellschaft für Mathematik und Datensysteme), who handles the registration for all German applications with a length up to 16 byte.

for Germany:

ID German National Registration Authority

c/o GMD, att. Mr. Bruno Struif

Rheinstrasse 75, 64295 Darmstadt, Germany

For the international registration of RIDs (registrated application provider identifiers = AID) a provider should - according to ISO 7816, part 5, chapter 7 - apply to the standard body of his related country. So every country should have such an organization like the GMD in Germany, which signs responsible. In the absence of such body or organization the secretariat of the ISO technical body is responsible for the assignment.

7.3 AP

The application personalizer identifier is optional.

7.4 Proprietary AIDs

For very small applications or pilot projects not registered AIDs can be used. Bits 5 to 8 of the first AID byte at address “0x15” must be set to logic 1. This means, the AID has to start with “F”, to indicate, that it is not registered.

Major constraint with unregistered AIDs: there is no guarantee that application IDs do not overlap!

7.5 ATR-file

The ATR-file is coded in the same way as the DIR-file, as already explained above, and contains information about the IC manufacturer, the IC-type (so for instance 0x05 stands for PCx2032, 0x15 stands for PCF2042) and the serial number of the card.

7.6 Short ATR

The ATR within the PCF2006 payphone/debit card IC is just a so called “short ATR”. It is 16 bytes long and is stored in the lower partition of the memory (this ATR is not defined by ISO).

Main purpose is also to identify the card to the terminal.

The codes currently used have to be applied and are assigned an organization called ProElectron.

The whole procedure and the contents bases on an agreement of the main smart card IC manufacturer and system providers.

Contents of the ATR reflects the following information:

- IC manufacturer
- IC type
- Card maker
- application code

The code is not transparent, but can be traced back.

The major target is here as well to distinguish between different applications.

All IC maker now are members at ProElectron and are accordingly prepared, the card manufacturers have not got active yet. (The number itself might be given to preference, but there is no guarantee.)

The total memory area from address 0 to 23 is write protected and read only when delivered. PS programs the ATR, Fab data and fab key (transport code, 24 bit) during final test and sets all bits in card data and some of the count data to “1”.

8 FABKEY PROCEDURE

According to ISO 7816 Philips delivers the Memory Card ICs initially programmed. Some of the first 32 byte of the Main Memory area, e.g. the ATR header, have to be programmed and write protected.

In addition to the Standard Order Entry Form the customer fills in an extra form, the FabKey Order Entry Form. By this the initial content of

- the first 32 byte of the Main Memory area,
- the Protection Memory and
- the Security Memory (Reference Data)

is specified. This set of data is called the FabKey of the Memory Card ICs, e.g. for the PCF2042 - 39 byte. The Philips FabKey procedure controls the handling of the FabKey specified by the customer.

8.1 Filling in the FabKey Order Entry Form

The FabKey Order Entry Form consists of two sections:

- General section (customer name, arrangements, FabKey verification) and
- FabKey data table.

The second line of the FabKey Order Entry Form, field Customer, asks for the name of the company. The remaining fields of this line are intended for internal handling and should be left blank.

Next some options can be selected:

Table 3 FabKey Order Entry Form

No.	ITEM		COMMENT
1	Customer delivers FabKey via	q file: diskette q file: data transfer q FabKey data table	
2	Data valid for	q 1 diffusion batch only q n batches, n = q all batches	
3	Customer data file is	q 1 record q more than 1 record	
4	Encryption RSA key file name: Philips Customer	q yes	

No. 1: How to send the FabKey data to Philips. One of three transfer media can be selected.

No. 2: Assignment of FabKey data to order quantities. The standard option is to specify one data set only (by file or data table) that is applied to **all batches**, i.e. the ordered quantities. On customer demand each unit of approximately 75.000 dies (one batch) can be programmed individually. For this the customer has to deliver a sufficient number of data sets (by file), where each data file is valid for **1 diffusion batch only**. Option **n batches, n =** is a feature that gives the freedom to the customer for individual assignments of FabKey data. For this the comment field should be used.

No. 3: Structure of customer data file. Data files for the Memory Card ICs are **1 record** only. Option **more than 1 record** is reserved.

No. 4: Encryption. For maximum security encryption via RSA may be selected. Two pairs of RSA-keys are needed for data transfer.

The FabKey data may be specified by file (diskette or data transfer) or using the FabKey data table in the FabKey Order Entry Form. In any case all 39 byte are expected in hexadecimal notation, e.g.

DATA NO.	ADDRESS (HEX.)	DATA (HEX.)															
1 to 16	00 - 0F	A2	13	10	91	FF	FF	82	15	FF	FF	FF	FF	FF	FF	FF	FF
17 to 32	10 - 1F	FF	FF	FF	FF	FF	F0	01	02	03	04	FF	FF	FF	FF	FF	FF
33 to 36 (1)	Bits 0 - 1F	30	FF	1F	FC	Protection Memory											
37 to 39	Bytes 1 - 3	FF	FF	FF	Security Memory												
-	20 - FF	data not defined via FabKey															

Note

1. The LSB of data no. 33 corresponds to bit address 0 of the Protection Memory and to byte address 0 of the Main Memory. Respectively the LSBs of data no. 34, 35, 36 correspond to byte addresses 8, 16, 24 of the Main Memory.

8.2 Verification of the FabKey

To ensure correct data transfer between customer and Philips, standard option is the verification of the FabKey data. When the FabKey is entered by Philips it is locked until it has been verified by the customer. For this the customer signs a FabKey Verification Form and returns it back to Philips to unlock the FabKey for production.

8.3 Further questions

There is a software package available that supports the customer in creating data records, verification of FabKey data, and encryption/decryption via RSA.

For more details to the FabKey Procedure contact Philips.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Supply voltage	-0.3	+6.0	V
V_I	Input voltage	-0.3	+6.0	V
P_{tot}	Power dissipation		70	mW
T_{stg}	Storage temperature range	-40	+125	°C

10 DC CHARACTERISTICS

According to ISO 7816-3; T_{amb} = -40 to +85°C (PCF2042).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		4.5	5.5	V
I_{DD}	supply current		-	10	mA
V_{IH}	input voltage HIGH (I/O, CLK, RST)		3.5	V_{DD}	V
V_{IL}	input voltage LOW (I/O, CLK, RST)		0	0.8	V
I_{IH}	input current HIGH (I/O, CLK, RST)		-	50	µA
I_{IL}	output current LOW (I/O)	V_{IL} = 0.4 V, note 1	0.5	-	mA
V_{LI}	leakage current (CLK, RST)	$V_{IL} = V_{DD}$, note 1	-	±10	µA
I	leakage current HIGH (I/O)	$V_{IH} = V_{DD}$, note 1	-	10	µA

Note

1. Open drain output.

11 AC CHARACTERISTICS

T_{amb} = -40 to +85°C (PCF2042).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
f_{CLCL}	External clock frequency	-	7	52	kHz
t_{CHCX}	Clock high period	-	8.6	-	µs
r_{CLK}	Clock pulse ratio	at 52 kHz	40	60	%
t_{CLCH}	Clock rise time	-	-	1	µs
t_{CHCL}	Clock fall time	-	-	1	µs
$t_{HD; STA}$	Hold time for START condition	-	4	-	µs
$t_{SU; STA}$	Set-up time for START condition	-	4	-	µs
$t_{HD; DAT}$	Data hold time	-	1	-	µs
$t_{SU; DAT}$	Data set-up time	-	1	-	µs
$t_{SU; STO}$	Set-up time for STOP condition	-	4	-	µs
t_{RES}	RESET pulse width	-	14	-	µs
t_E	EEPROM erase time	at 51.2 kHz	2.5	-	ms
t_W	EEPROM write time	at 51.2 kHz	2.5	-	ms
t_R	EEPROM data retention time	T_{amb} = 55 °C	10.0	-	yrs
$N_{E/W}$	EEPROM endurance (number of erase/write cycles)	t_E = 2.5 ms; t_W = 2.5 ms	100000	-	cycles
C	I/O; RESET; CLK pin capacitive	T_{amb} = 25 °C	-	10	pF

12 ESD PROTECTION

T_{amb} = -40 to +85°C (PCF2042).

TEST CONDITION	RESULT
ESD Human Body model Q22, 22°C; note 1	5 kV
ESD machine model Ford; note 1	200 V
ESD machine model Philips; note 1	300 V

Notes

1. Discharge procedure according ISO/IEC 10373:1993 (E) point 6.4.2 Procdure and 6.4.3 Result

13 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

14 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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